UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,714	07/15/2003	David J. Corisis	108298532US1	9586

25096 7590 08/02/2006

PERKINS COIE LLP
PATENT-SEA
P.O. BOX 1247
SEATTLE, WA 98111-1247

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,714	CORISIS, DAVID J.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *51-55,57-60,62,64,65,67,69-72,74,76,77,84 and 85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *51-55,57-60,62,64,65,67,69-72,74,76,77,84 and 85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/620714 Attorney's Docket #: 108298532US1
Filing Date: 7/15/2003;

Applicant: Corisis

Examiner: Alexander Williams

This application is a divisional application of serial number 09/644766, filed 8/23/2000, now U.S. Patent # 6,607,937.

Applicant's Amendment filed 6/13/06 to the Applicant's election of species of figure 3 (claims 50-55, 57-74, 76 and 77), filed 6/29/04, has been acknowledged.

This application contains claims 56, 75 and 78-83 drawn to an invention non-elected without traverse in Paper No. 4. A complete response to the final rejection must include cancellation of non-elected claims or other appropriate action (see 37 CFR ∋ 1.144 & MPEP ∋ 821.01).

The indicated allowability of claims 52, 53, 61, 66, 69-72, 74, 76 and 77 are withdrawn in view of the newly discovered reference(s) to Pao and Schaper. Rejections based on the newly cited reference(s) follow.

Claims 1-50, 63, 68 and 73 have been canceled.

Claims 62 and 77 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 62 and 77 recites the limitation "the microelectronic substrate" in the claim. There is insufficient antecedent basis for this limitation in the claim.

Any of claims 62 and 77 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 52, 53, 51, 54, 55, 57-60, 62, 69-72, 74, 76, 77, 84 and 85, **insofar as claims 62 and 77 can be understood**, are rejected under 35 U.S.C. 102(b) as being anticipated by Pao (U.S. Patent # 5,386,343).

52. Pao (figures 1 to 63) specifically figure 2 show a packaged microelectronic devices, comprising: a support member **10** having support member circuitry; a first packaged

microelectronic device **20** connected **(by 22)** to at least one of the support member and the support member circuitry and having a first microelectronic die **(inherent)** generally encased in a first encapsulant **(inherent)** to define a first package configuration; and a second packaged microelectronic device **26** connected **(by 28)** to at least one of the support member and the support member circuitry with the first packaged microelectronic device positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device having a second microelectronic die **(inherent)** generally encased in a second encapsulant **(inherent)** to define a second package configuration different than the first package configuration, and wherein the second package microelectronic device is not fixedly attached to the first packaged microelectronic device, wherein the first package microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third adage, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

53. Pao (figures 1 to 63) specifically figure 2 show a packaged microelectronic devices, comprising: a support member **10** having support member circuitry; a first packaged microelectronic device **20** connected **(by 22)** to at least one of the support member and the support member circuitry and having a first microelectronic die **(inherent)** generally encased in a first encapsulant **(inherent)** to define a first package configuration; and a second packaged microelectronic device **26** connected **(by 28)** to at least one of the support member and the support member circuitry with the first packaged microelectronic device positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device having a second microelectronic die **(inherent)** generally encased in a second encapsulant **(inherent)** to define a second package configuration different than the first package configuration, and wherein the second package microelectronic device is not fixedly attached to the first packaged microelectronic device, wherein the first package microelectronic device has a first planform shape in a plane generally parallel to a plane of the support member and the second package microelectronic device has a second planform shape in a plane generally parallel to the plane of the support member, and

further wherein the second planform shape is more extensive in at least one direction generally parallel to the plane of the support member than is the first planform shape.

51. The assembly of claim 50, Pao further comprising a conductive connecting member **28** connected directly between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to an outer edge of the first packaged microelectronic device.

54. The assembly of claim 50, Pao show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.

55. The assembly of claim 50, Pao show wherein the second packaged microelectronic device has a plurality of conductive members **28** electrically coupled to the second microelectronic die and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry without being attached to the first packaged microelectronic device.

57. Pao (figures 1 to 63) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **10**; a first packaged microelectronic device **20** connected to the support member and having a first microelectronic die **(inherent within 20)** generally encased in a first encapsulant **(inherent)** to define a first planform shape; and a second packaged microelectronic device **26** connected to the support member with the first packaged microelectronic device positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device having a second microelectronic die **(inherent within 26)** generally encased in a second encapsulant **(inherent)** to define a second planform shape different than the first planform shape.

58. The assembly of claim 57, Pao show wherein the support member **10** defines a support member plane and the first planform shape describes an area in a first plane generally parallel to the support member plane that is smaller than an area described by the second planform shape in a second plane generally parallel to the support member plane.

59. The assembly of claim 57, Pao further comprising a conductive connecting member **28** connected directly between the second packaged microelectronic device and the

support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.

60. The assembly of claim 57, Pao show wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge and the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

62. The assembly of claim 57, Pao show wherein the second packaged microelectronic device has a plurality of conductive members **28** electrically coupled to the microelectronic substrate and extending away from the second encapsulant, further wherein all the conductive members extending away from the second encapsulant are attached directly between the second packaged microelectronic device and the support member circuitry.

70. Pao (figures 1 to 63) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **10** having support member circuitry; a first packaged microelectronic device **20** including a first microelectronic die **(inherent within 20)** electrically coupled directly to the support member circuitry, wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge; and a second packaged microelectronic device **26** including a second packaged microelectronic device **(inherent within 26)** electrically coupled directly **(by 28)** to the support member circuitry without any direct electrical connections to the first packaged microelectronic device, the first packaged microelectronic device being positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device, the second packaged microelectronic device having a third edge and a fourth edge facing opposite the third edge, and wherein the third edged of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

69. The assembly of claim 70, Pao further comprising an elongated conductive connecting member **28** connected between the second packaged microelectronic device and the support member circuitry, at least a portion of the connecting member being positioned adjacent to the first packaged microelectronic device.
71. The assembly of claim 70, Pao show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.
72. the assembly of claim 70, Pao show wherein the first packaged microelectronic device is electrically coupled to the second packaged microelectronic device via the support member circuitry.
76. Pao (figures 1 to 63) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **10** having support member circuitry; a first packaged microelectronic device **20** including a first microelectronic die **(inherent within 20)** electrically coupled directly to the support member circuitry, wherein the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge; and a second packaged microelectronic device **26** including a second packaged microelectronic device **(inherent within 26),** the second packaged microelectronic device being connected directly **(by 28)** to the support member with the first packaged microelectronic device being positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device not being fixedly attached to the first packaged microelectronic device, the second packaged microelectronic device having a third edge and a fourth edge facing opposite the third edge, and wherein the third edged of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.
74. The assembly of claim 76, Pao show wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the first and second packaged microelectronic devices.
77. The assembly of claim 76, Pao show wherein the second packaged microelectronic device has a plurality of conductive members electrically coupled to the microelectronic substrate and extending away from an encapsulant of the second microelectronic device, further wherein all the conductive members extending away from the

encapsulating of the second microelectronic device are attached directly between the second packaged microelectronic device and the support member circuitry.
84. Pao (figures 1 to 63) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **10**; a first packaged microelectronic device **20** connected to the support member and having a first microelectronic die **(inherent within 20)** generally encased in a first encapsulant **(inherent)** to define a first planform shape; and a second packaged microelectronic device **26** connected to the support member with the first packaged microelectronic device positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device having a second microelectronic die **(inherent within 26)** generally encased in a second encapsulant **(inherent)** to define a second planform shape different than the first planform shape, wherein the second packaged microelectronic device is spaced apart from the first packaged microelectronic device to define a gap between the packaged devices.
85. Pao (figures 1 to 63) specifically figure 2 show an assembly of packaged microelectronic devices, comprising: a support member **10**; a first packaged microelectronic device **20** connected to the support member and having a first microelectronic die **(inherent within 20)** generally encased in a first encapsulant **(inherent)** to define a first device footprint; and a second packaged microelectronic device **26** connected to the support member with the first packaged microelectronic device positioned between the support member **(bottom of 10)** and the second packaged microelectronic device **26**, the second packaged microelectronic device having a second microelectronic die **(inherent within 26)** generally encased in a second encapsulant **(inherent)** to define a second device footprint different than the first device footprint.

Claims 65, 64 and 67 are rejected under 35 U.S.C. 102(b) as being anticipated by Schaper (U.S. Patent # 6,707,680 B2).

65. Schaper (figures 1 to 8) specifically figure 1 show an assembly of packaged microelectronic devices, comprising: a support member **122**; a first packaged microelectronic device **126** having a first microelectronic die **(inherent within 126)** generally encased in a first encapsulant **(inherent)** and connected to the support

member with a plurality of solder balls **132**, the first packaged microelectronic device has a first edge and a second edge facing opposite the first edge; and a second packaged microelectronic device **120** having a second microelectronic die **(inherent within 120)** generally encased in a second encapsulant **(inherent)** and connected to the support member with a plurality of elongated connection members **(leads)** extending from the second packaged microelectronic device around at least part of the first packaged microelectronic device and attached directly to the support member, the second packaged microelectronic device has a third edge and a fourth edge facing opposite the third edge, and wherein the third edge of the second packaged microelectronic device extends outwardly beyond the first edge of the first packaged microelectronic device and the fourth edge of the second packaged microelectronic device extends outwardly beyond the second edge of the first packaged microelectronic device.

64. The assembly of claim 65, Schaper show wherein the first packaged microelectronic device includes a first surface facing toward the support member, a second surface facing away from the support member and toward the second packaged microelectronic device, and a plurality of third surfaces between the first and second surfaces, further wherein the elongated connection members **(leads)** are positioned adjacent to the third surfaces of the first packaged microelectronic device.

67. The assembly of claim 65, Schaper show wherein the support member includes support member circuitry, and further wherein all the elongated connection members **(leads)** of the second microelectronic device are attached directly to the support member circuitry.

Response

Applicant's arguments filed 6/13/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678,e25.013,e23.092,e25.023,e23.052,e23.004,e 23.069,e23.075 365/63,51	8/31/04 3/29/05 9/8/05 3/4/06 7/26/06
Other Documentation: foreign patents and literature in 257/686,685,777,723,737,734,738,778,779,772,666,673, 668,687,678,e25.013,e23.092,e25.023,e23.052,e23.004,e 23.069,e23.075 365/63,51	8/31/04 3/29/05 9/8/05 3/4/06 7/26/06
Electronic data base(s): U.S. Patents EAST	8/31/04 3/29/05 9/8/05 3/4/06 7/26/06

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
7/27/06

Primary Patent Examiner
Alexander O. Williams